

FIGURE 1D

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FIGURE 1E

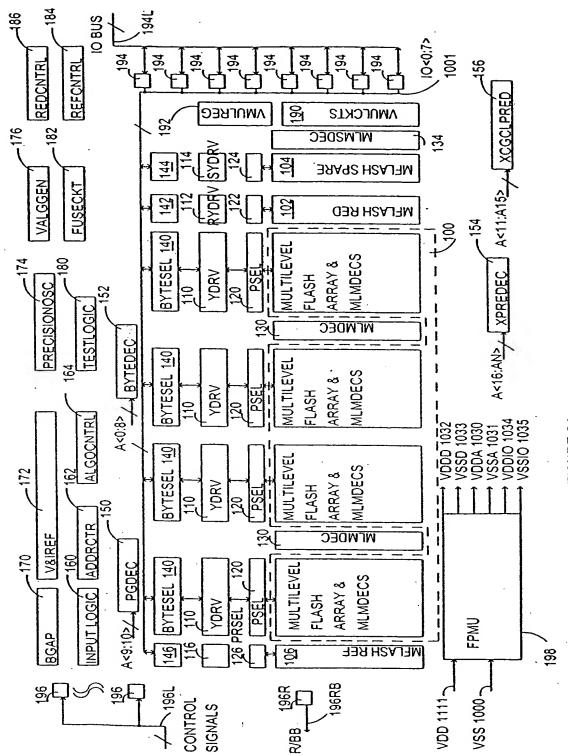
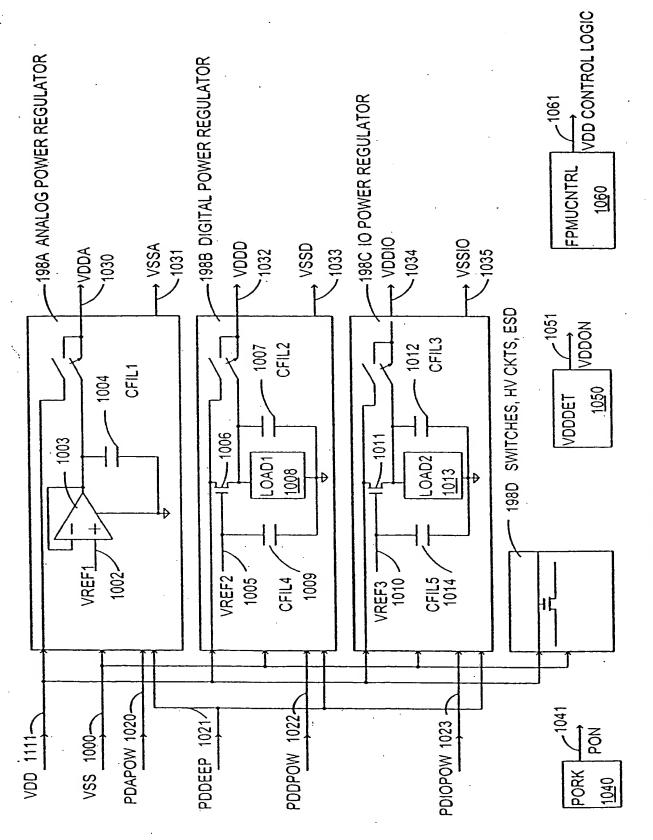
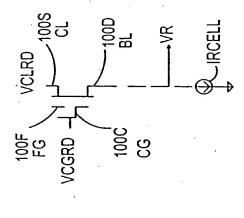


FIGURE 2A



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FIGURE 2B



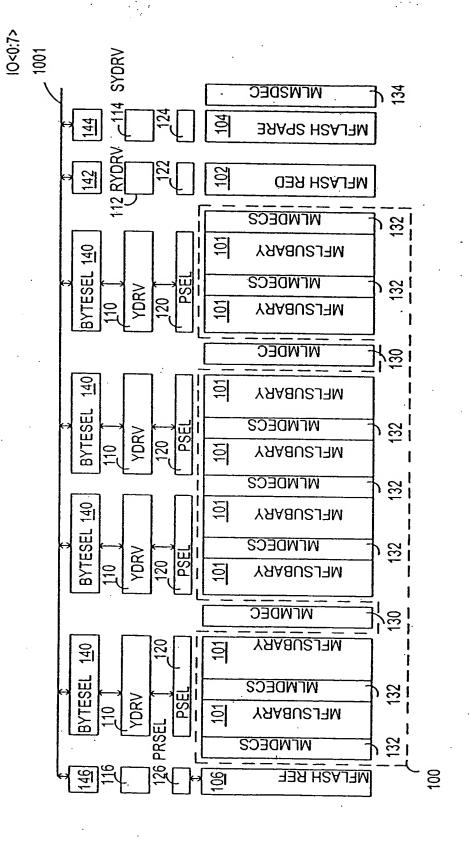
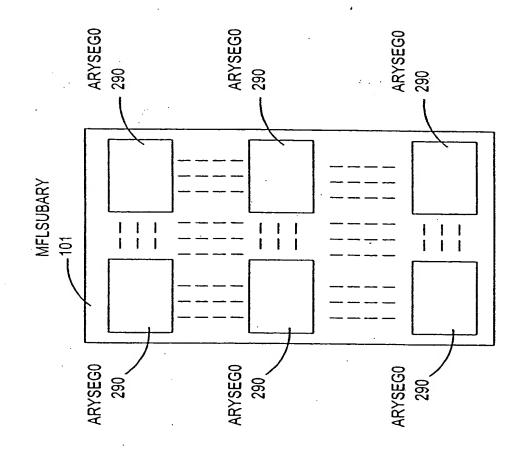
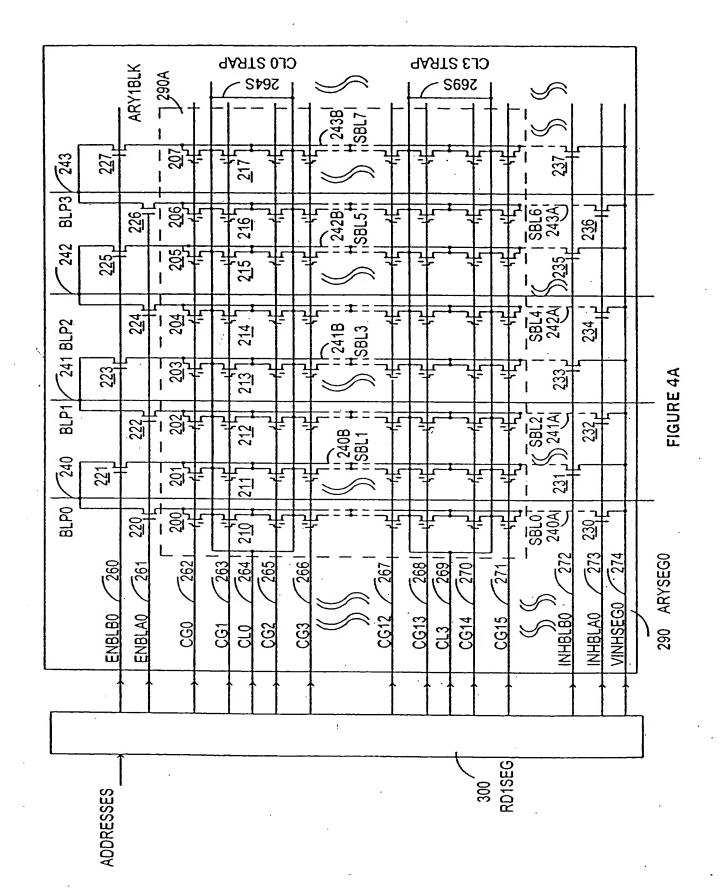
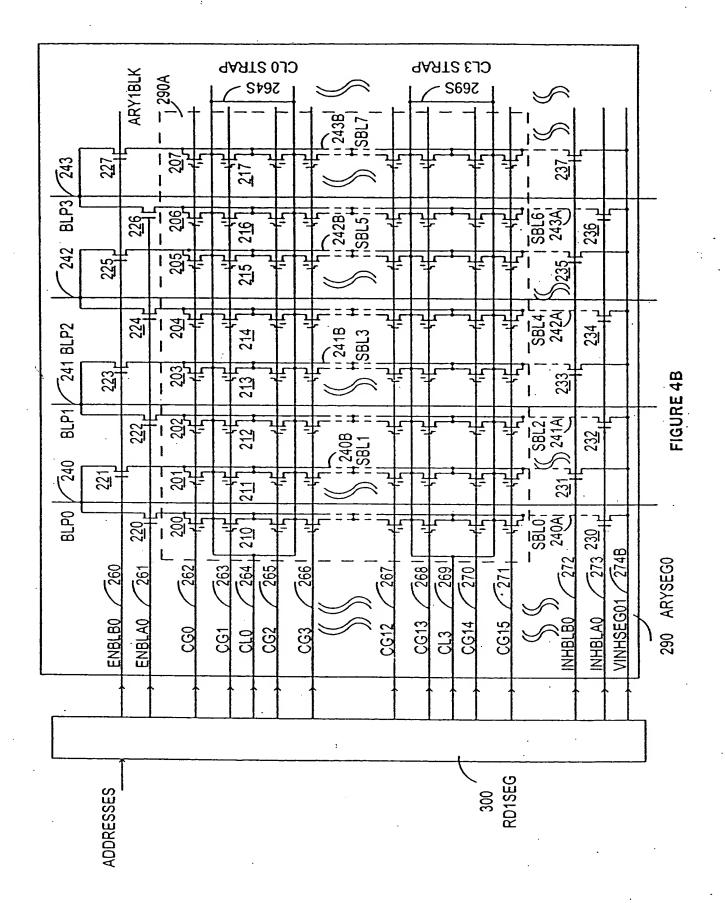
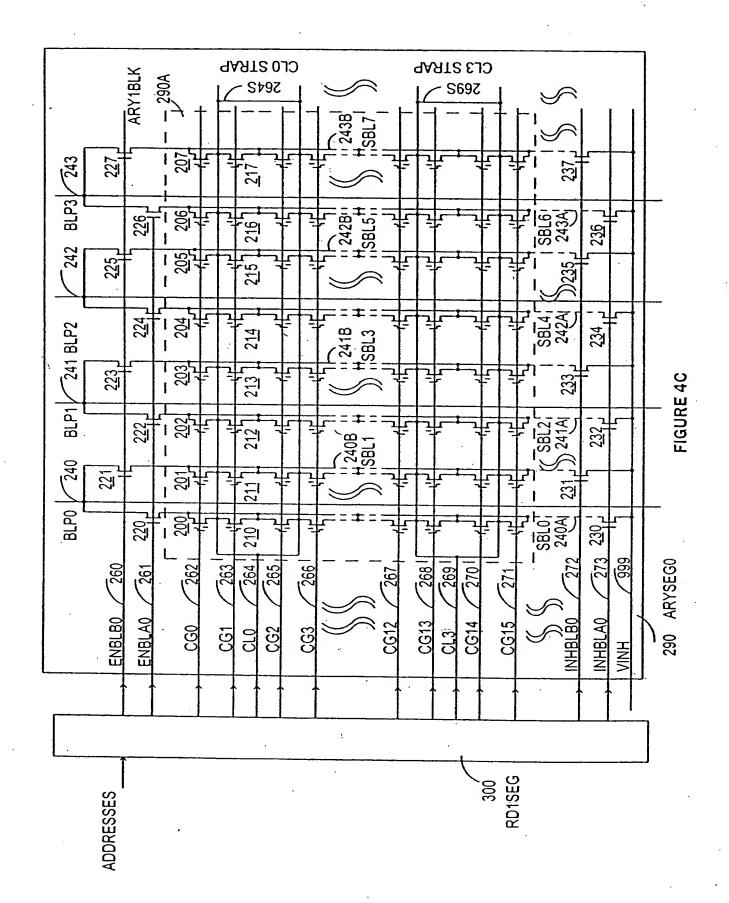


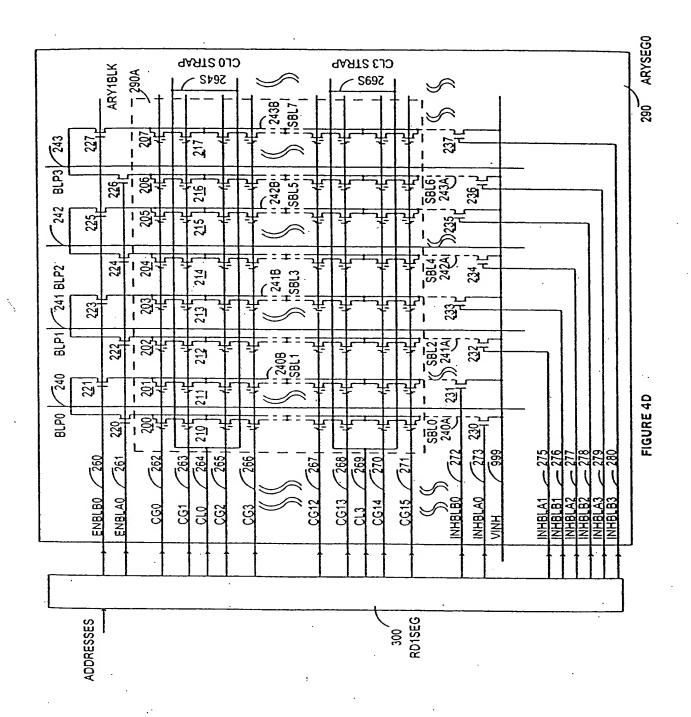
FIGURE 3B

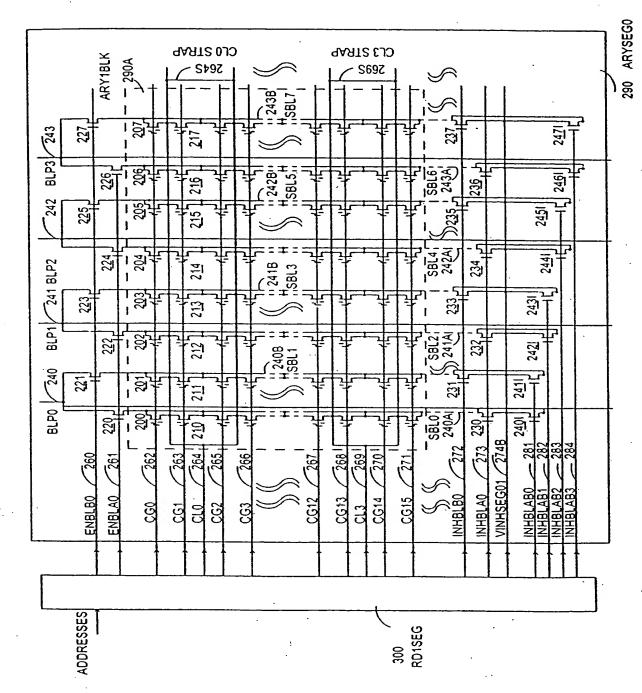












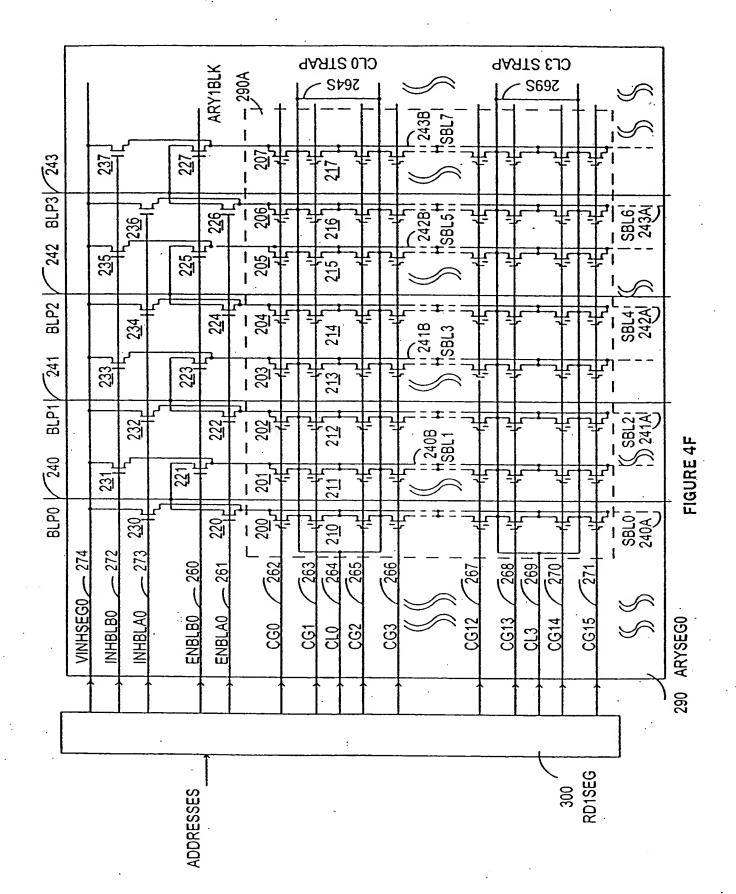


FIGURE 5A

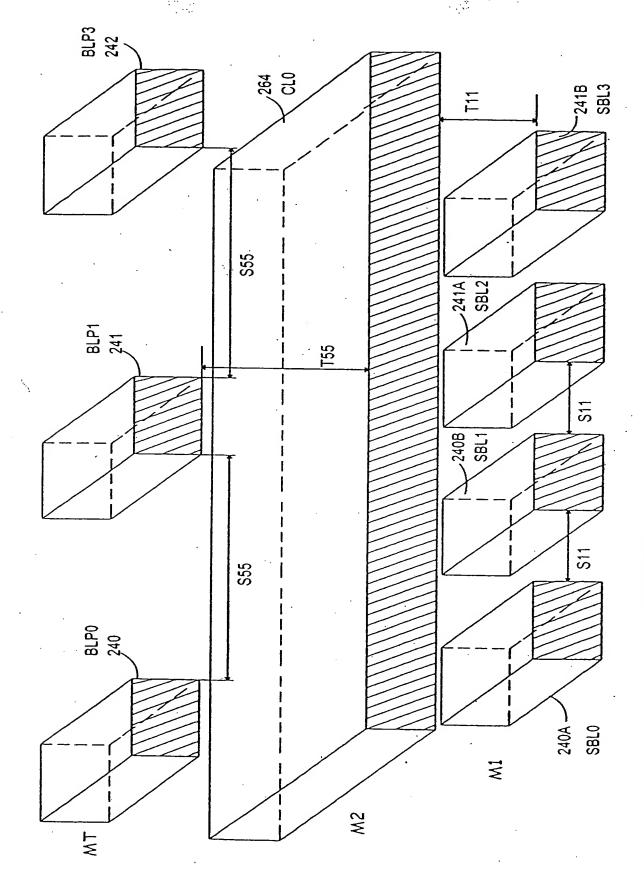
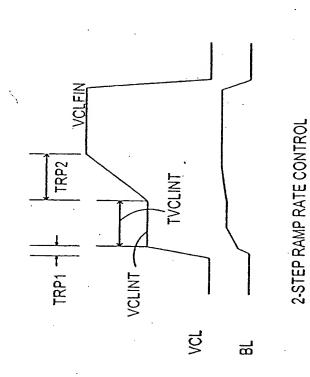
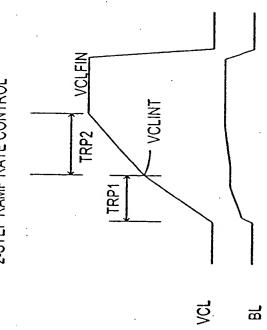


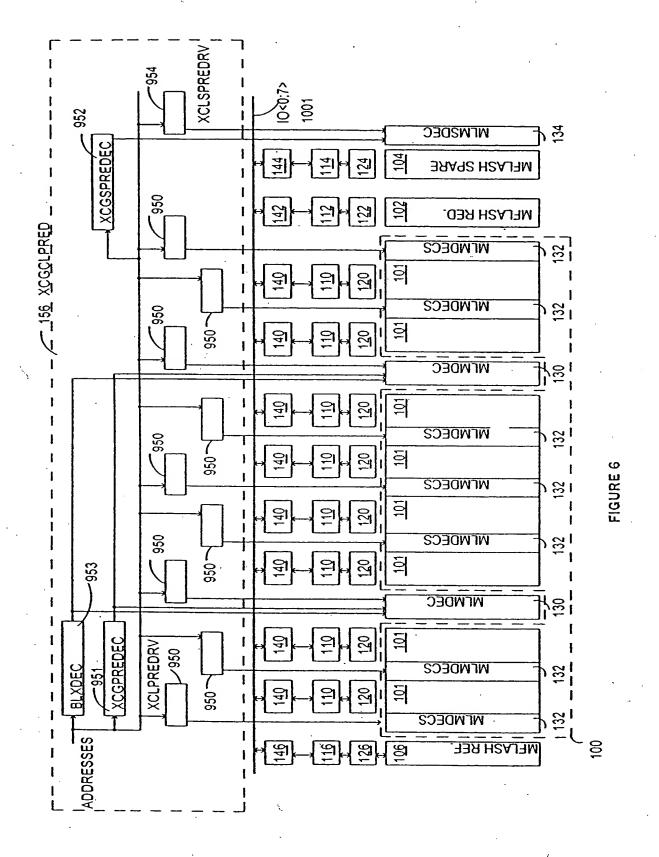
FIGURE 5B





FAST-SLOW RAMP RATE CONTROL

FIGURE 5C



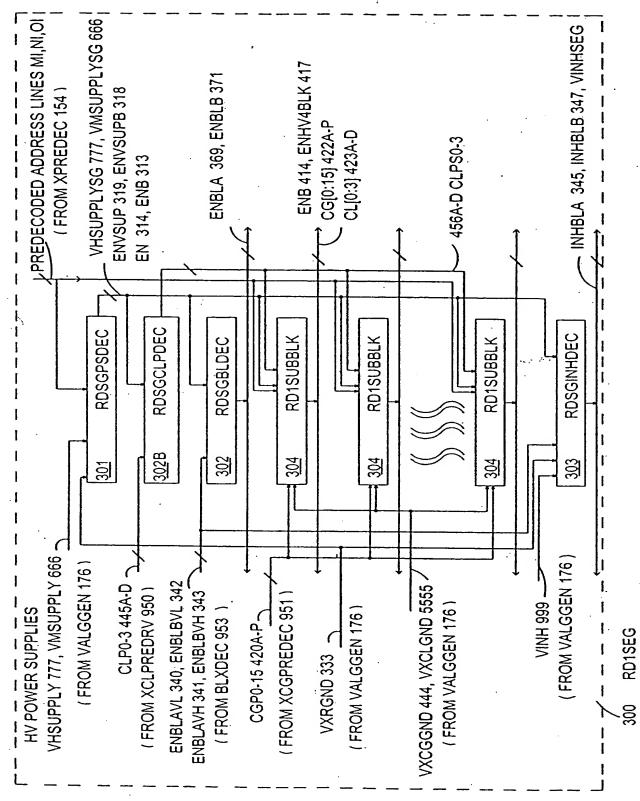
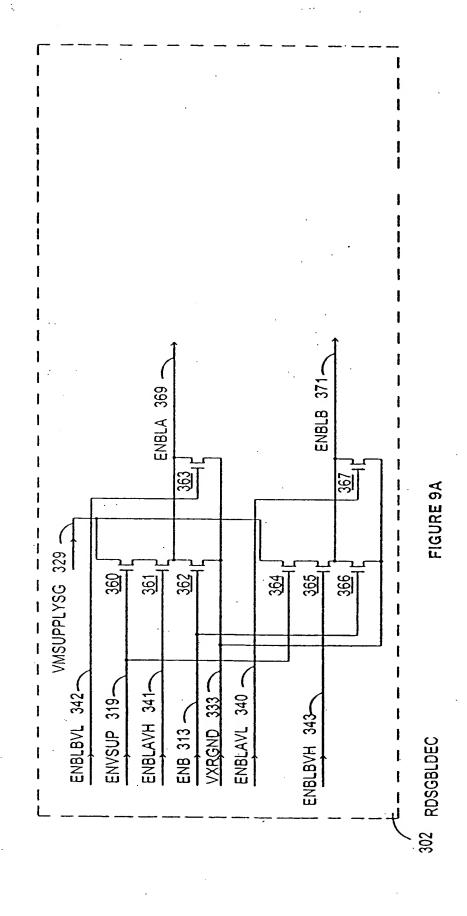
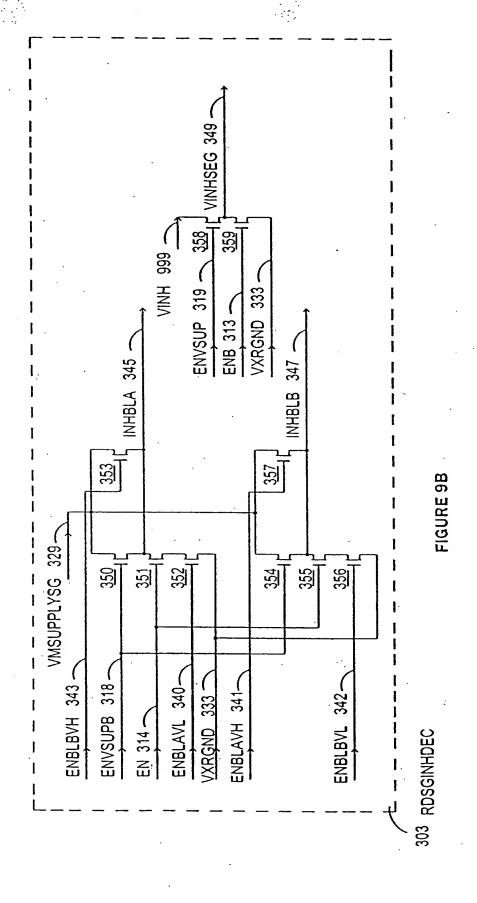


FIGURE 7

FIGURE 8





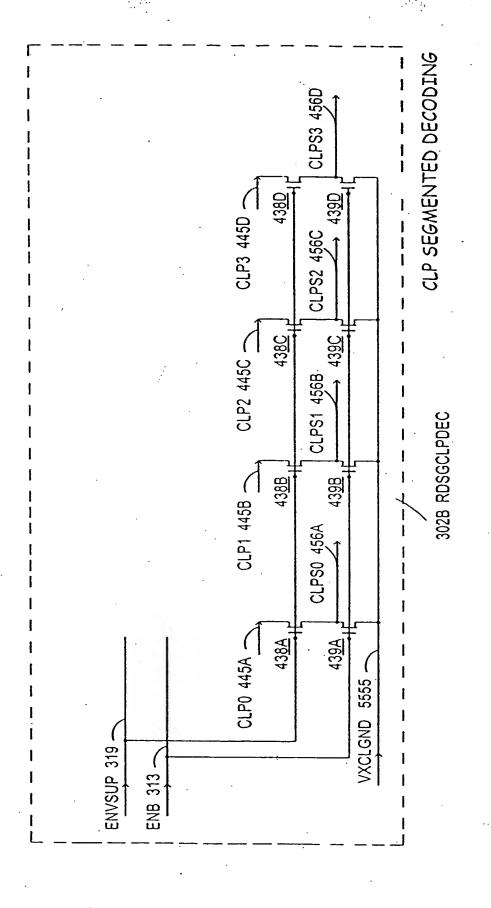


FIGURE 90

FIGURE 10

FIGURE 11A

FIGURE 11B

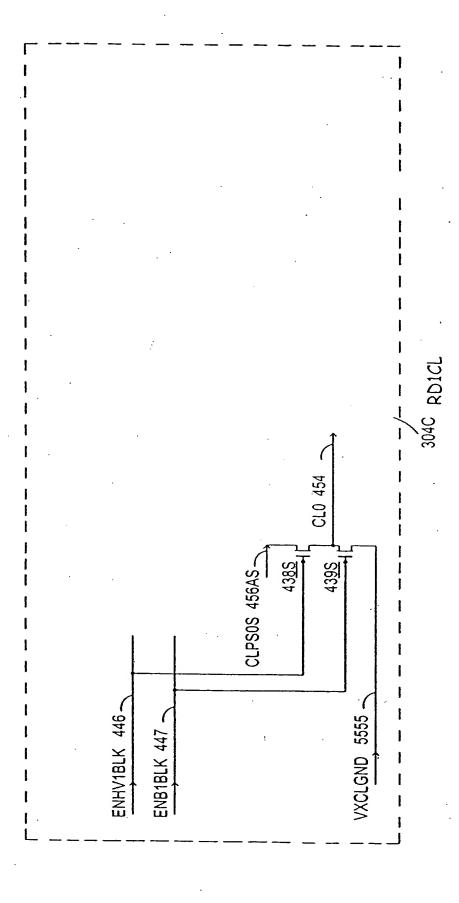


FIGURE 11C

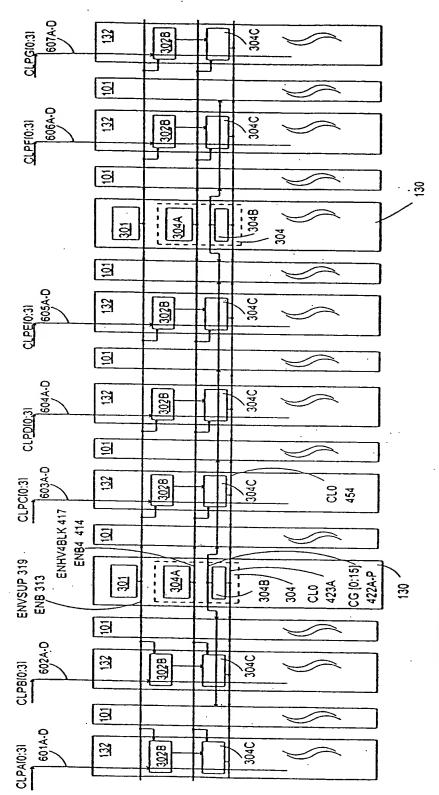


FIGURE 12

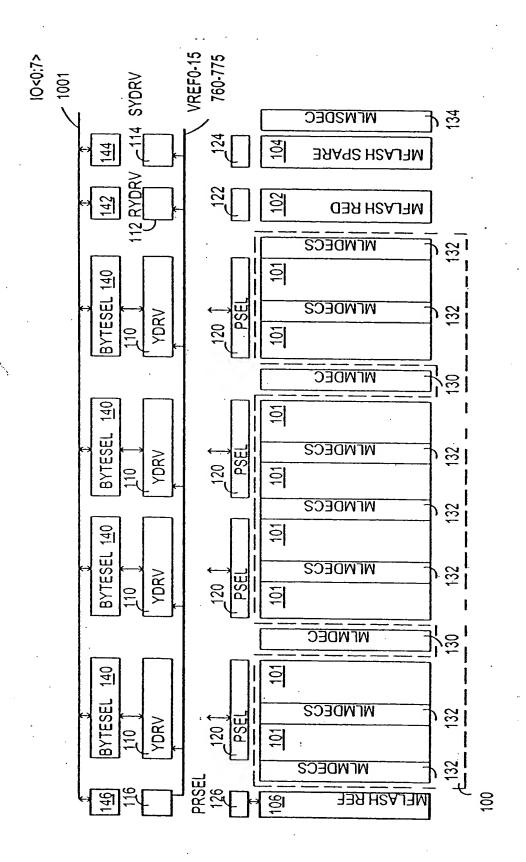
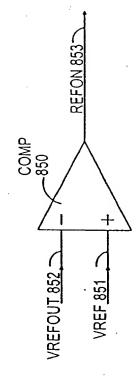


FIGURE 14



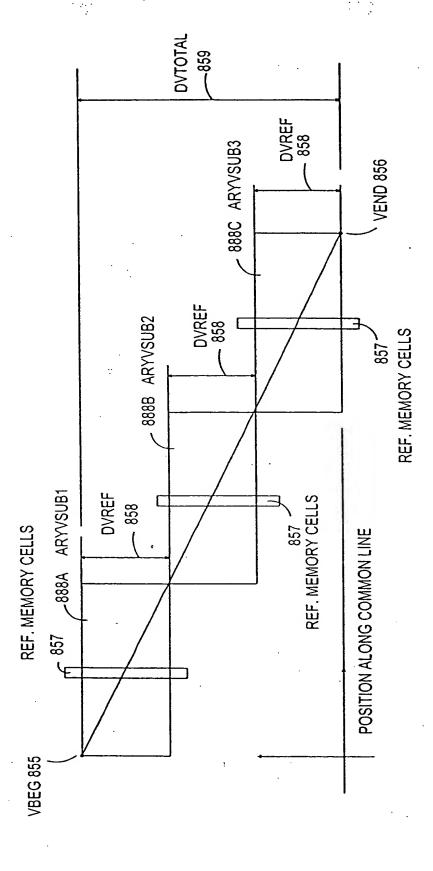


FIGURE 16

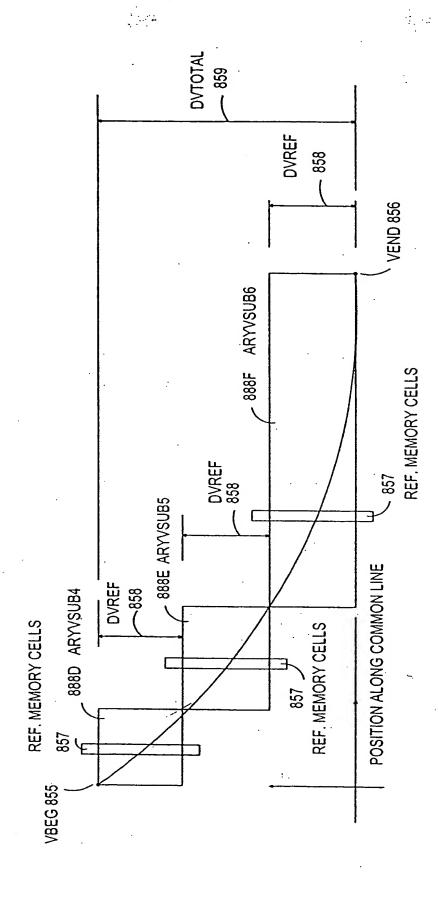


FIGURE 17

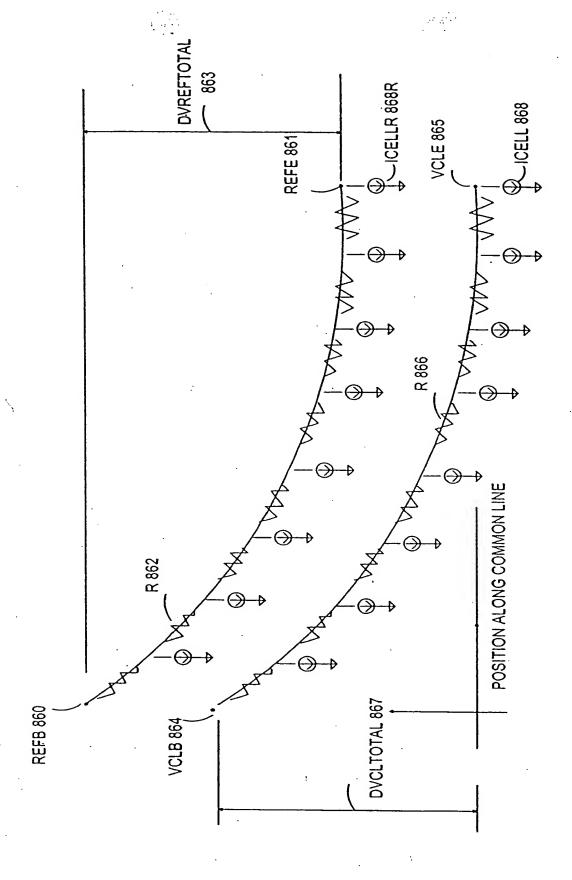


FIGURE 18

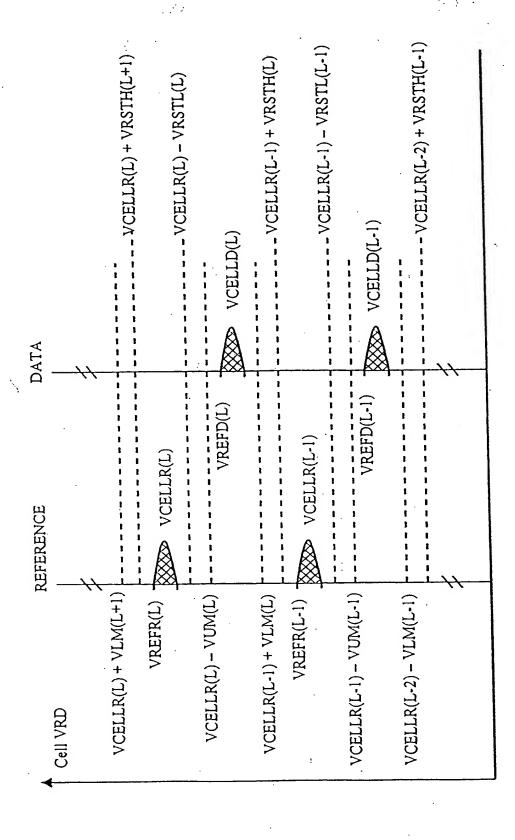


FIG. 194

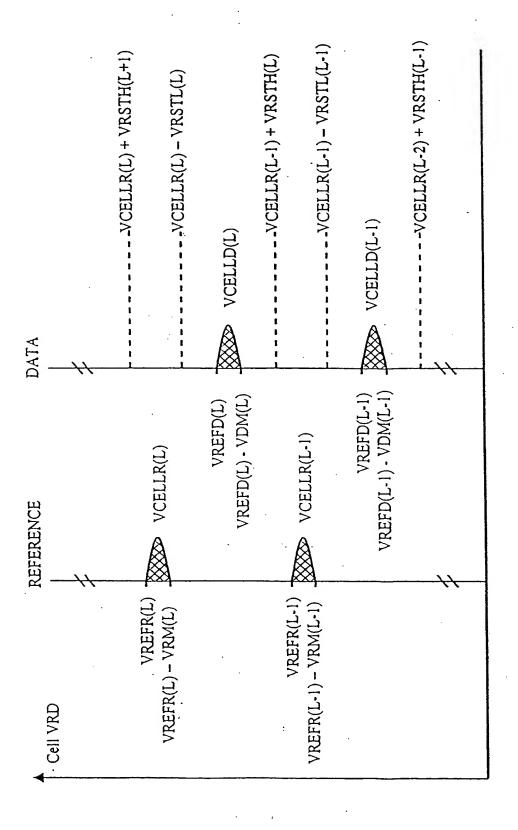
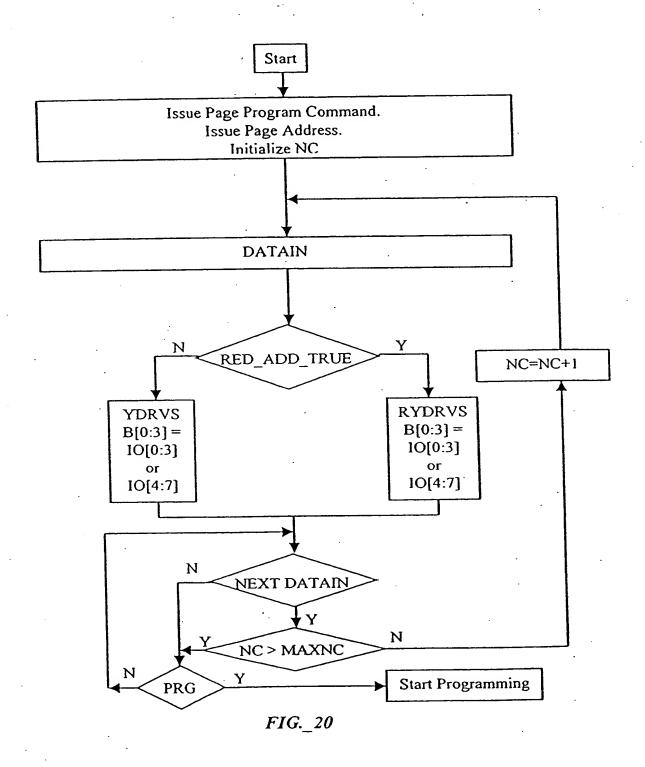
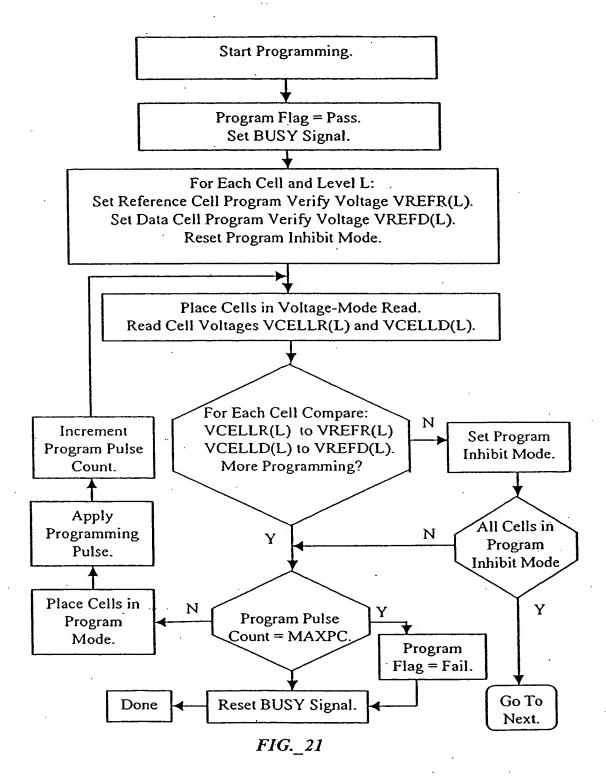


FIG._19B





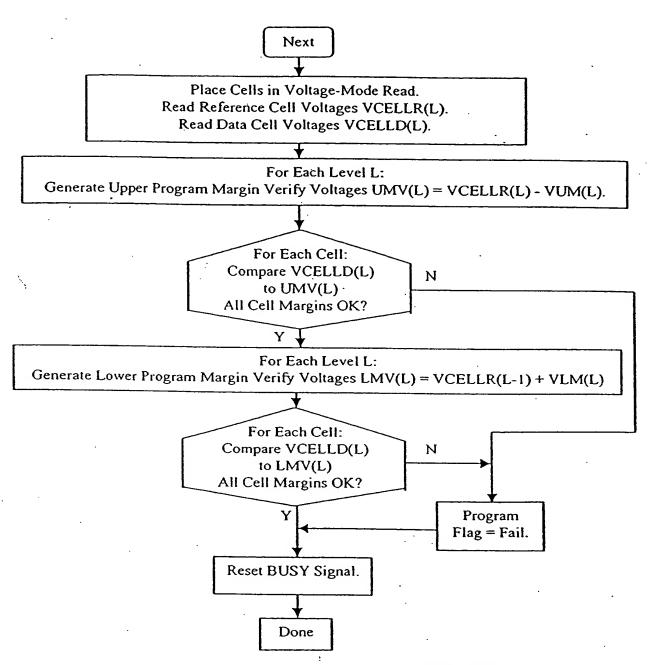


Fig._22A

Next

Place Cells in Voltage-Mode Read.

Read Reference Cell Voltages VCELLR(L).

Read Data Cell Voltages VCELLD(L).

For Each Level L:

Generate Program Margin Verify Voltages RMV(L) = VREFR(L) - VRM(L)& DMV(L) = VREFD(L) - VDM(L)

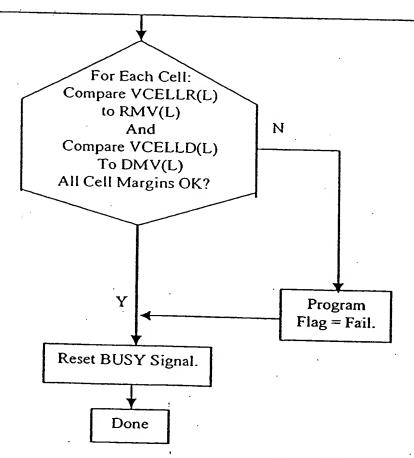
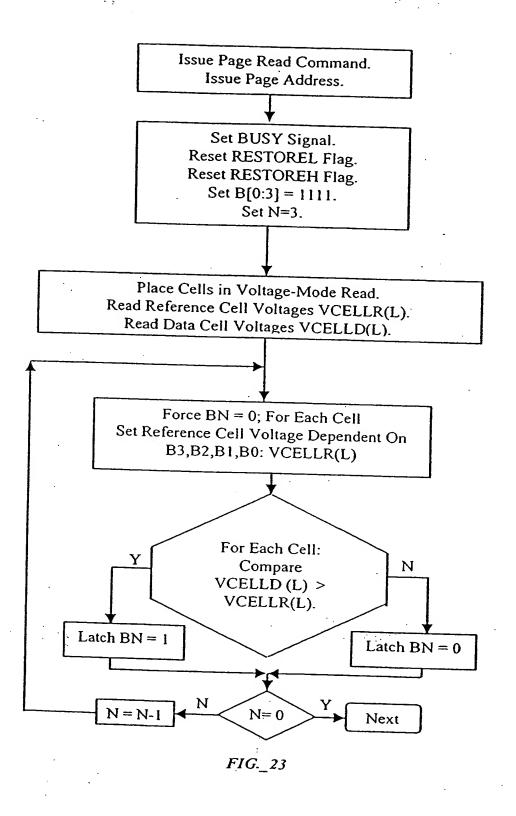


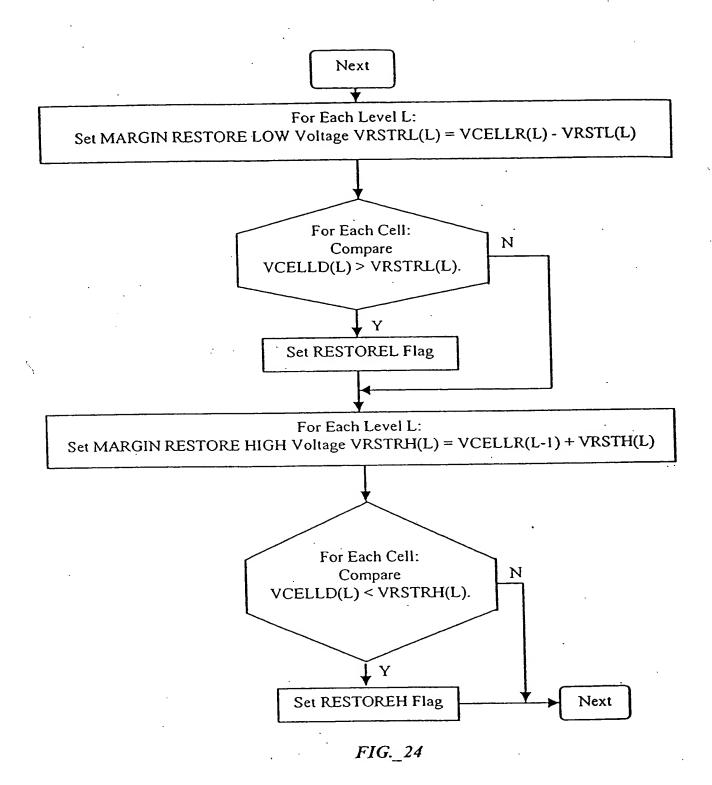
Fig._22B

Next Place Cells in Voltage-Mode Read. Read Reference Cell Voltages VCELLR(L). Read Data Cell Voltages VCELLD(L). For Each Level L: Generate Program Margin Verify Voltages RMV(L) = VREFR(L) - VRM(L) & DMV(L) = VREFD(L) - VDM(L)For Each Cell: Compare VCELLR(L) to RMV(L) And Ν Compare VCELLD(L) To DMV(L) All Cell Margins OK? BSERV Program Flag = Fail. Reset BUSY Signal.

FIGURE ZZC

Done





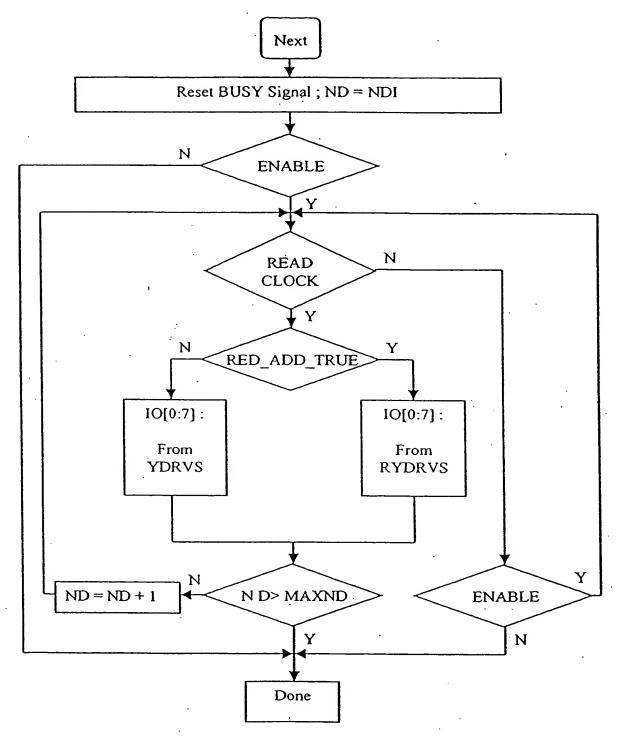


FIG._25

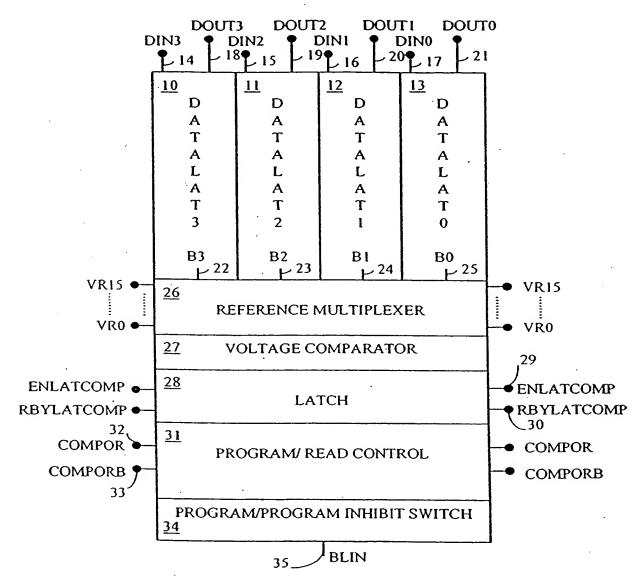
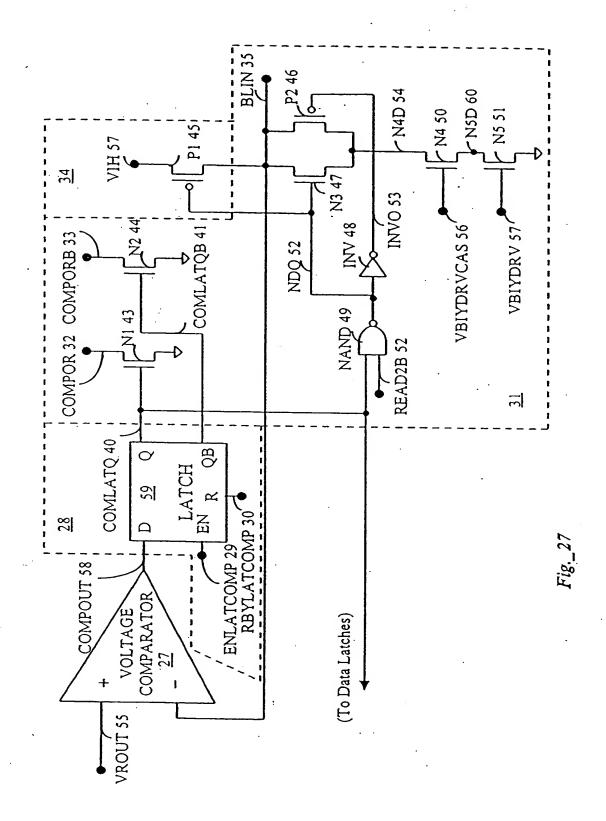
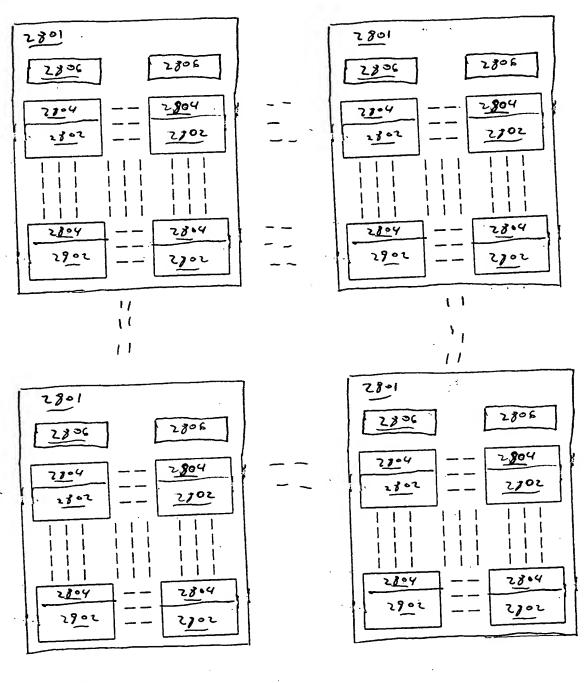


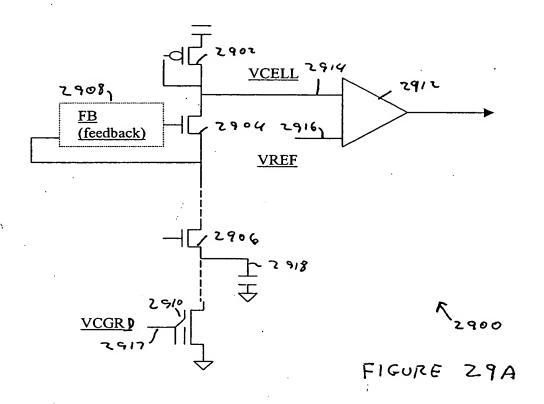
Fig._26

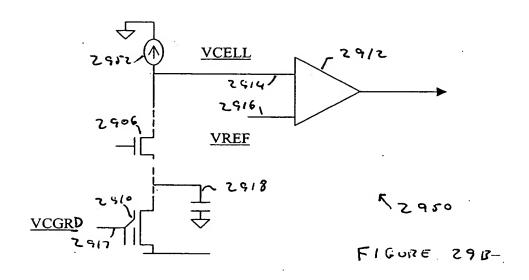




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FIGURE 28





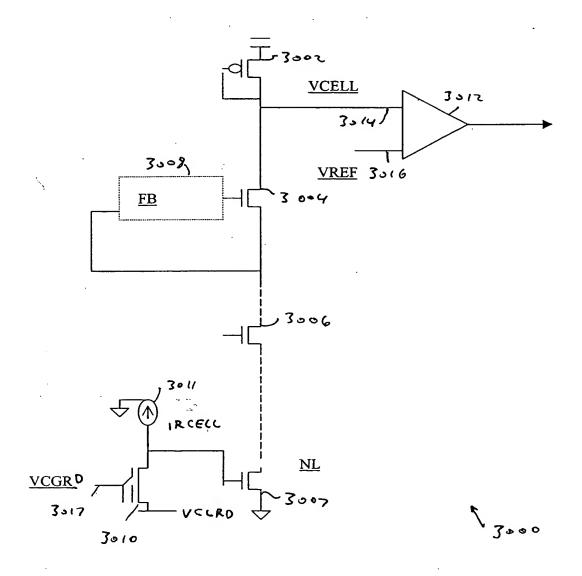


FIGURE 30

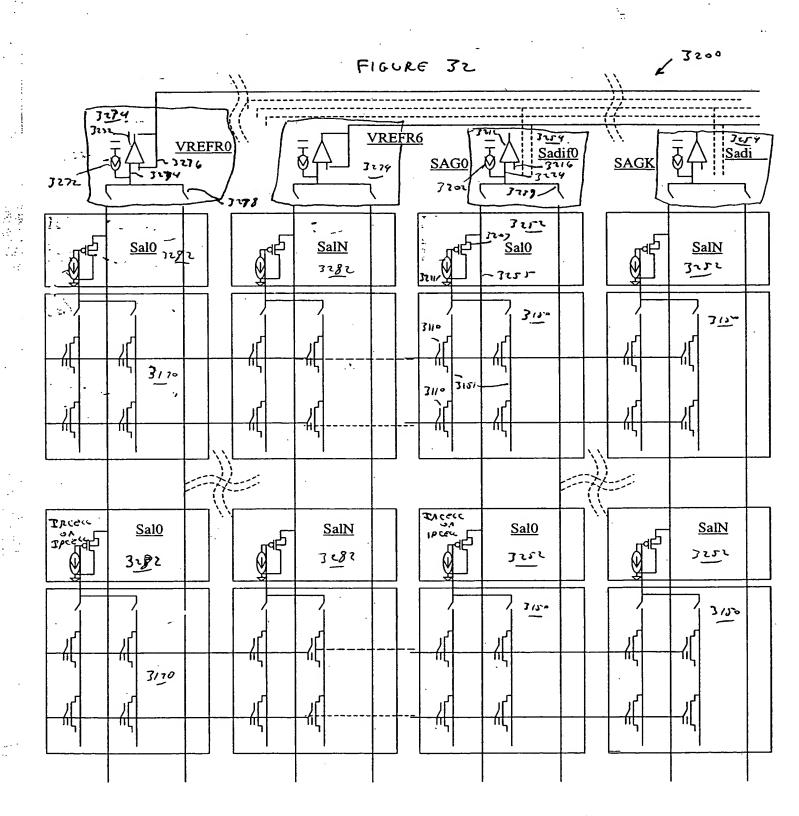
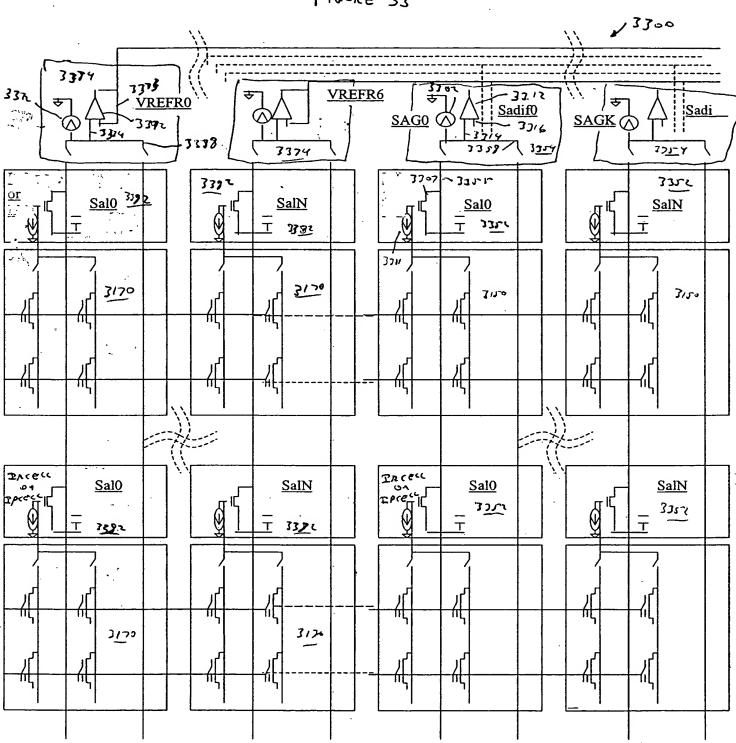


FIGURE 33



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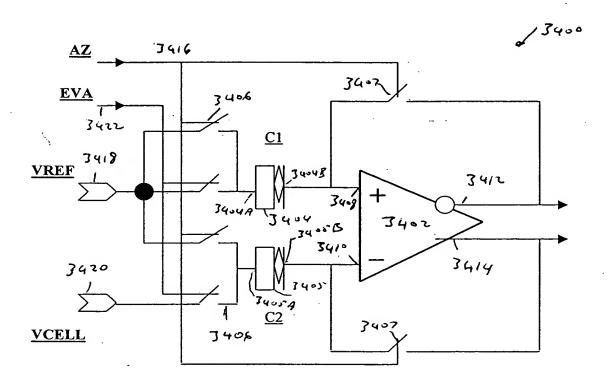


FIGURE 34

